DESIGN ADVISER SOLUTION SUGGESTIONS

Comprehensive Data for all designers. For specifics see the EMC results details where results are color coded, those in green causing less problems and in yellow for those that should be resolved and finally in red for those needing critical attention. Note however there is interaction or Side Effects for some rules.

100.1 Closed Loops, Open Loops Rule Book **Differential Mode**

Rule Justification A tracking loop constitutes a loop antenna for EMI. Radiation is generated in the plane of the loop.

Rule Description The area, frequency of operation and signal amplitude on each loop are determined. The severity of each loop is determined from these parameters.

Possible Actions

1. Re-route the net to reduce the loop area
2. Reduce the edge rate of the signal driving the loop

Possible Side-Effects on Other Rules

1. Track Length
2. XY Tracking

100.2 Track Shielding Rule Book Differential Mode

Rule Justification A surrounding shield provides a local return path for EMI.

Rule Description High-speed tracking is checked for the presence of shielding as specified by the net-shield net attribute. If present, this attribute contains the name of the required shielding net. For nets with this attribute, the rule checks for surrounding shield tracks. The ideal situation is that the entire tracking for the net has planar shielding on both sides.

Possible Actions Introduce a surrounding shield as specified by the net-shield attribute

Possible Side-Effects on Other Rules None

100.3 Impedance Profile Rule Book Differential Mode

Rule Justification In order to reduce EMI and susceptibility it is good policy to attempt to reduce inductance and increase capacitance in the signal tracks. The characteristic impedance of a line is approximately the square root of L/C, so high impedance areas are an indication that additional capacitance is required.

Rule Description Tracks are checked for approximate characteristic impedance, and tracks exhibiting a high impedance compared to the remainder of the tracks on a layer are highlighted. The results are frequency and edge-speed weighted so that the problem is considered more severe on faster signals.

Possible Actions

1. Introduce a ground plane if none is present.
2. Reduce the dielectric thickness between the signal and ground/power planes.
3. Introduce partial ground areas on signal layers adjacent to affected tracks.
4. Make affected tracks wider provided that the impedance obtained is compatible with the driver technology.

Possible Side-Effects on Other Rules

1. Layer Stack

2. Track Shielding

100.4 XY Tracking Rule Book Differential Mode

Rule Justification In multi-layer boards, adjacent signal layers should be routed primarily in opposite directions, with one layer primarily in the X direction and the adjacent layer primarily in the Y direction. For EMI it helps to reduce EM field reinforcement by avoiding parallel-running tracks on adjacent layers. If this rule is not followed, severe cross-talk is also likely to result.

Rule Description The degree to which tracking is primarily in the X and Y directions is determine for each signal layer. The result reflects the degree to which each layer is routed in the required direction. The results are also frequency and edge-speed weighted so that the greater severity of the problem on higher-speed signals is recognized. The degree of X/Y tracking on a layer is determined as a ratio of the total run length in the X and Y directions. However, only routed segments over a given length are highlighted. (The minimum length is weighted by the edge-speed of the net.) It is possible, where there are a lot of shorter segments, to have an incorrectly biased layer with no highlighted segments. The layer will still be indicated as having an incorrect bias.

Possible Actions

1. If the design has been auto-routed, check that the router has been set up with the correct directional bias on each layer. If not, re-routing may be necessary.
2. To make less major improvements, use the highlighting feature to determine the most problematic wrong-way routes to see if improvement can be obtained manually.

Possible Side-Effects on Other Rules

1. Track Length
2. Open Loops
3. Closed Loops
4. Impedance Profile

100.5 Design Adviser Suggestion Stubs

Rule Justification: Stubs are branches from the main signal path. When stubs are over a certain length, they can cause distortion due to signal reflections.

Rule Description: The maximum stub delay is specifiable as a design parameter which limits the stub delay as a fraction of the signal transition time. The design parameter is Max Stub Delay. A report is generated which lists the nets in error only. Nets on which an error occurs are highlighted in the Attention color.

Suggestion:

1. Shorten the routed stub length.
2. Use a driver with a slower rise time.

100.6 Track Resonance Rule Book Differential Mode

Rule Justification If the time-length of a route approaches a multiple of a quarter of the wavelength of its signal (or a harmonic), its efficiency as an antenna, and hence radiation, can be increased.

Rule Description The known frequency of operation of the signal, and the known rise time are used to

derive a set of significant frequencies where quarter-wave-length tuning is important. If the time-length of a route approaches the quarter-wavelength time, the net containing the route is highlighted. Ninety percent resonance gives a red high-light, while amber is shown at eighty percent. Terminated nets are always considered to be satisfactory.

Possible Actions

1. Re-route the net
2. Use a slower driving component

Possible Side-Effects on Other Rules

1. Track Length
2. Open Loops
3. Closed Loops
4. Track Stubs

100.7 Return Loops Rule Book Differential Mode

Rule Justification Signals and their return paths form loops which cause radiated emissions.

Rule Description Each signal is checked for a ground or power return within the shielding distance specified as a design level parameter. Coplanar or adjacent layer shielding is allowed. Nets are highlighted in the Attention color if less than 45 percent of the net has a return path within the required distance, or Caution color if less than 95 percent.

Possible Actions Use a partial power plane to introduce a return path

Possible Side-Effects on Other Rules None

100.8 Layer Stack Rule Book Common Mode

Rule Justification On any design using high-speed components, atleast one ground plane should exist to ensure reasonable control of emissions. The existence of a ground plane also ensures that the characteristic impedance of lines is well-defined and is effective in suppression of excessive inter-line crosstalk. For the purposes of EMI suppression, the ideal placement for ground and power planes is on the external board layers. This is often impractical from a manufacturing viewpoint.

Rule Description The placement of power and ground planes with respect to signal tracks is analyzed to determine what proportion of the signal tracking is shielded above and below by power or ground planes. The greater this proportion, the higher the reading on the analysis meter.

Possible Actions 1. If no ground planes exist If it is permissible to introduce ground and power planes rather than routed signals, then this is highly desirable on a highspeed design. Ideally, these planes should be placed on outer layers, since they act as an EMI shield. If a ground plane may not be introduced due to cost or other factors, then consider grounding via a grid pattern with a wide ground track around the periphery of each layer. Place ground fill areas underneath high-speed components and in void areas wherever possible. Shield high speed lines with ground tracks.

2. If at least one ground plane exists The ideal placement is to have a ground plane on each outer layer, and to avoid stacking signal layers together with no intervening ground plane. This is not always possible due to cost and manufacturing constraints.

Possible Side-Effects on Other Rules

1. Track Shielding
2. Open Loops
3. Closed Loops
4. XY Tracking
5. Impedance Profile
6. Plane Impedance
7. Overlapping Planes

100.9 Isolated Areas Rule Book Common Mode

Rule Justification The practice of using partial ground plane areas for screening purposes can cause isolated conductor areas to exist. These can then act as secondary radiators. There is already a check available for this in the layout tool.

Rule Description The rule checks that all copper areas are physically connected to a signal. The severity of the problem is in proportion to the copper area in each case. This rule relies on the results of a previous batch check having been generated in Layout.

Possible Actions Ground or remove the affected area

Possible Side-Effects on Other Rules

1. Track Shielding
2. Impedance Profile

100.10 Overlapping Power Planes Rule Book Common Mode

Rule Justification It is bad practice to overlap non-corresponding power planes as this leads to undesirable noise current distribution throughout the system.

Rule Description Areas of non-corresponding plane overlap are detected between layers. The severity of the problem is proportional to the total overlap area.

Possible Actions Remove areas of overlap

Possible Side-Effects on Other Rules

1. Track Shielding
2. Isolated Areas

100.11 Component Placement Rule Book Common Mode

Rule Justification Placing the highest speed/power components in close proximity to the power source reduces power plane transient problems. For boards without ground planes, radiation from power tracks is reduced.

Rule Description For each component which drives a net with a net-class attribute, the speed of operation and output voltage transition is determined. The relative placement of components with respect to the point of entry of the power source for each component is assessed, and the ideal placement region for each class of component is calculated. Components falling outside their ideal dis tance from their power source are highlighted.

Possible Actions Move component

Possible Side-Effects on Other Rules

All rules concerned with signal tracking

100.12 Component Decoupling Rule Book Common Mode

Rule Justification Appropriate decoupling of components is essential to reduce trasient conditions on supply connections. It is possible to calculate the required decoupling capacitor value.

Rule Description Each component is checked for correct decoupling as specified in the decoupling data file. A report is generated listing components in error. Incorrectly decoupled components are highlighted in the Attention color if the decoupling is missing or separated from the decoupled pins by more than twice the required distance. The Caution color is used if the decoupler is between the correct distance and twice that distance away from the component.

Possible Actions Insert a decoupling capacitor of the required value

Possible Side-Effects on Other Rules None

100.13 Power Plane Impedance Rule Book Common Mode

Rule Justification A ground or power plane may become excessively perforated by component pins, via holes and cutouts in a concentrated area. The effect of this is twofold: Firstly, the pure resistance of the plane is increased in the affected area and secondly the impedance is increased. The effect of this is that unwanted transient conditions may exist on the plane leading to increased emissions.
Rule Description Each plane is divided into a number of areas, each of which is analyzed for excessive perforation when compared to the other areas.
Possible Actions

1. Increase the plating thickness on affected power planes
2. Use the smoothing function to reduce via perforation

Possible Side-Effects on Other Rules Tracking-dependent rules

100.14 Termination Rule Book Fast Circuit

Rule Justification Signal reflections cause extra high-frequency harmonics to be generated. Each line has a critical length over which reflections are a maximum and below which they are reduced. It is good practice to terminate lines which are close to the critical length.
Rule Description The line delay is determined for each signal path which starts at a driver pin (determined by the pin's data_type or by the pin having a pin_order attribute value equal to the source pin order for the net's net class). Where the net is unrouted, the delay is estimated according to the route lengths. The rise time of the signal is known via characteristics associated with the net class. Correct termination is assumed if any component on a net is identifiable as a terminator (for discrete components,this means having an elec_type attribute with value "res", "cap", "ind" or "dio"), and the component is placed correctly. For unterminated nets, the proportion of the critical length is determined. The most problematic nets are highlighted.
Possible Actions

1. Terminate the line with an appropriate termination network. If the termination class has been set for the net in question it is possible to do this automatically.
2. Attempt to shorten the routed length on Other Rules

1. Track Length
2. Closed Loops
3. Open Loops
4. Track Stubs

100.16 Track Length Rule Book Fast Circuit

Rule Justification Long routes, particularly at high frequencies and edge-rates, generate EMI and also affect susceptibility.
Rule Description Each route is checked for ideal (by Manhattan Distance) and actual length. The result is frequency and edge-speed weighted so that results deteriorate as the ratio of actual to ideal length and the frequency and edge speed increase.
Possible Actions Naturally, it is desirable to attempt to reduce the tracking
Possible Side-Effects on Other Rules None

100.18 Crosstalk Rule Book Fast Circuit

Rule Justification Crosstalk causes noise to be coupled onto parallel-running signal tracks. This can cause false triggering and reduces the noise margin.
Rule Description Using the results from the field solver rule, the coupling between lines is determined. This is combined with the known transition voltage and rise time of the active signal to determine the resulting crosstalk voltage at the passive net receiver. Terminations are taken into account by the analysis, provided that terminators have a comp_type attribute with value 'term'. Termin ators are assumed to terminate perfectly. A report is generated listing the predicted combined crosstalk voltages on each net, with the contributions from parallel running signals on the same and immediately adjacent layers. Nets exceeding the value specified in the net attribute net_max_xtalk, or the design level parameter 'Max Crosstalk' are highlighted in the Attention color.
Possible Actions
1. Move the lines further apart
2. Terminate the passive (victim) line at the receiver to reduce the crosstalk by as much as 50 percent
Possible Side-Effects on Other Rules None

100.19 Impedance Rule Book Fast Circuit

Rule Justification The track width required for each net on each layer is dependent on the required characteristic impedance.
Rule Description Each net is analyzed for the required track width on each layer.
The design level parameters are:
1. Default Zo

The board level default required impedance in Ohms. If this value is set to zero, there is no default.
2. Width Increment

The minimum value and minimum increment for track width in mm. The rule reports the nearest track width to obtain the required impedance with the given increment.
3. Zo Tolerance

The allowable variation (plus or minus) for impedance in Ohms. Each net may also have a char_Z attribute whose value specifies the required impedance in Ohms. A report is generated listing the required track widths for each net on each layer. This is the report which you can access via the "Report" button. Nets which cannot meet the required impedance with the given increment and tolerance are highlighted in red. A second report is generated which shows the capacitance of the tracks (<design>/adviser/reports/<version>/lc.rep).

100.20 Current Rule Book Fast Circuit

Rule Justification The current capacity must be calculated to ensure that sufficient line widths are used in the design.
Rule Description The widths for each net are calculated and derated according to MIL-STD-275C. A report is generated which lists the required line widths. The required current capacity is specified by default by the design level parameter 'Current Req', and on a per-net basis by the attribute 'current'. The design level parameter 'Width Increment' specifies the minimum change in width and the minimum width value to be used, so for instance a value of 0.005 gives a minimum track width of 0.005 mm, and calculates widths in multiples of this value only. The maximum allowable temperature rise is specified by the design-level parameter 'Max Temp Rise'. Nets which already contain routes with widths less than the calculated derated value before allowance for automatic soldering are highlighted in red.