CADSTAR Design Migration Tool Installation and Operation Guide

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1. Installation of software

The **CADSTAR Design Migration Tool** is supported with CADSTAR 12.0 and later releases.

The CADSTAR Design Migration Tool is currently distributed as a ZIP file containing the executable, licence, configuration and mapping files. In order to use the tool it is necessary to unzip the contents of this file into the CADSTAR programs directory. This is typically located at:

C:\Program Files\Zuken\CADSTAR 12.1\Programs

2. Installation of licenses

There are two licence files necessary to operate the CADSTAR Design Migration Tool.

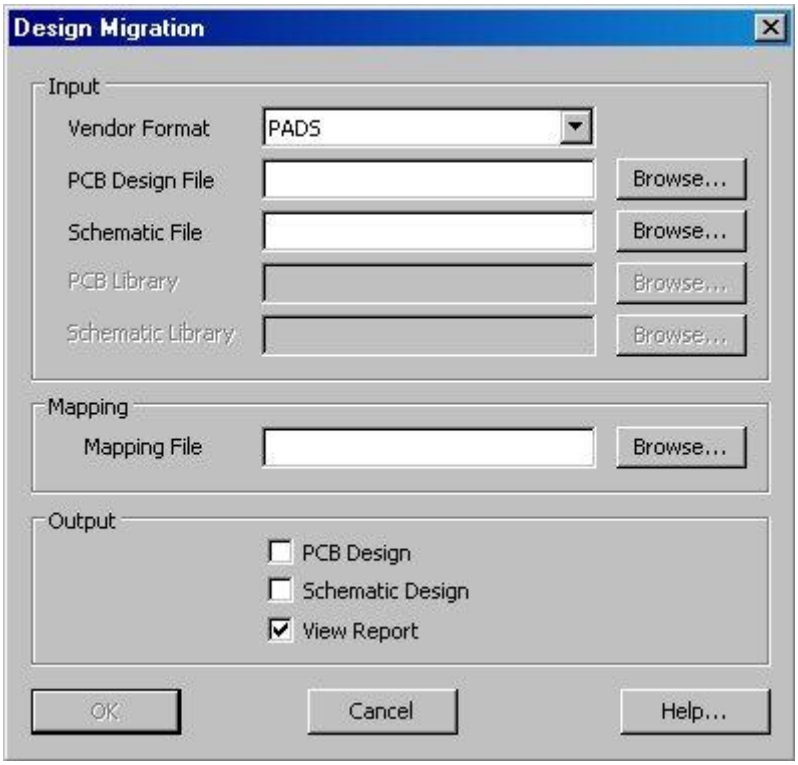
The primary license file will be supplied by Zuken through the normal authorization mechanism. Under normal circumstances you will be supplied with a complete license file containing all required license features (including the new one for the Design Migration Tool). However, if the license feature for the CADSTAR Design Migration tool is not already present in your existing CADSTAR license file and has been supplied separately, then this license feature must be manually appended to your standard Zuken license file. (If you are using a network license server, then the license server should be restarted).

An extra "generic" license file (named 'licenses.dat' – note the 's' on the end of 'licenses') is supplied in the ZIP file and must be placed in the same directory as the executable to enable operation of the vendor format readers. No license server or other configuration is required for this file. **Note: Please do <u>not</u> attempt to merge the contents of this license file into your standard CADSTAR license (e.g. license.dat) – it must remain as a separate file in the same folder as the executable.**

Note: The Design Migration menu and dialog will only be visible within CADSTAR when the software has been correctly installed and a valid license is available.

3. Basic operation

The CADSTAR Design Migration Tool is run from CADSTAR Design Editor. Selecting the **Design Migration** option in the **File** menu displays the following dialog.



To use the tool, first select the source **Vendor Format** from the option list.

Select the input PCB and Schematic design files. These will typically be the exported ascii files from the selected vendor. Please see **Appendix A** for details on the vendor formats and versions supported by the tool.

Note: The result of the design migration is usually more successful if both a matching, 'in-step' PCB and Schematic design are migrated together. This enables the tool to do additional consistency checking and makes sure that the migrated designs are in step. If PCB and Schematic designs are migrated independently then there could be possible inconsistencies in the resulting output designs.

In order for the tool to operate correctly, it is necessary to select a mapping file which will provide configuration settings and enable mapping of characters not supported in CADSTAR. For more information on the mapping file please see **Appendix B**.
Finally select the output required (PCB and/or schematic) and select OK to run the tool.

Note: Reading in additional input library information and automatically generating CADSTAR library data is not currently supported but will be implemented in a future release of the software.

The report output from the tool will be displayed (both during and optionally after the operation), along with any further messages generated by CADSTAR when the resulting designs are read in. Please see **Appendix C** for details of known issues and limitations of the tool.

Appendix A - Supported vendor formats/versions

1. PADS

The CADSTAR Design Migration Tool supports the migration of PADS design data from the PADS releases 5.0.1 and 2007.

To import PADS schematic design data, it is required that the user generates the PADS PowerLogic ASCII Design Export file.

To import PADS layout design data, it is required that the user generates a PADS-POWERPCB DESIGN DATABASE ASCII output file for the PCB board.

Directory structure	Description
<path>/<design>/<design>.txt	<path> : any path to the design directory <design> : name of the design directory <design> : name of the PADS PowerLogic ASCII Design Export file
<path>/<design>/<design>.asc	<path> : any path to the design directory <design> : name of the design directory <design> : name of the PADS PowerPCB DESIGN DATABASE ASCII file

2. OrCAD

The CADSTAR Design Migration Tool supports the migration of Cadence OrCAD design data from the OrCAD releases 9.1 and 9.2.

To import Cadence OrCAD schematic design data, it is required that the user generates an EDIF design file.

To import Cadence OrCAD Layout layout design data, it is required that the user generates a Cadence OrCAD Layout MIN Interchange output file for the PCB board.

Directory structure	Description
<path>/<design>/<design>.edf	<path> : any path to the design directory <design> : name of the design directory <design> : name of the EDIF Design Export file
<path>/<design>/<design>.min	<path> : any path to the design directory <design> : name of the design directory <design> : name of the Cadence OrCAD Layout MIN Interchange output file

3. P-CAD

The CADSTAR Design Migration Tool supports the migration of P-CAD design data from the release P-CAD 2006.

To import P-CAD schematic design data, it is required that the user generates a P-CAD V16 ASCII Schematic file.

To import P-CAD layout design data, is required that the user generates a P-CAD V16 ASCII Layout file.

Directory structure	Description
<path>/<design>/<design>.sch	<path> : any path to the design directory <design> : name of the design directory <design> : name of the ASCII schematic file
<path>/<design>/<design>.pcb	<path> : any path to the design directory <design> : name of the design directory <design> : name of the ASCII PCB layout file

4. Protel

The CADSTAR Design Migration Tool supports the migration of Protel design data from the Protel releases Protel98 and Protel99.

To import Protel schematic design data, it is required that the user generates for all existing blocks of the schematic design ASCII output files (*.asc files).

Note: For Protel99 it may be necessary to rename the generated file “Copy of <sheet>.prj” or “Copy of <sheet>.sch” into “<sheet>.asc”.

To import Protel layout design data, it is required that the user generates an ASCII output file (*.PCB file) for the PCB board.

Directory structure	Description
<path>/<design>/<project|sheet>.asc	<path> : any path to the design directory <design> : name of the design directory <project|sheet> : name of the ASCII schematic project or sheet file
<path>/<design>/<board_ascii>.pcb	<path> : any path to the design directory <design> : name of the design directory <board_ascii> : name of the ASCII PCB board file

5. Altium Designer

Although the CADSTAR Design Migration Tool does not provide a direct migration for Altium Designer data, it is still possible to migrate design data from Altium Designer by exporting in P-CAD or Protel formats.

When migrating layout design data from Altium Designer it is recommended that the P-CAD format (rather than Protel) is used as an intermediate format. However there are limitations in the P-CAD data output from Altium Designer that will affect the migration. Please see the section in Appendix C for details.

When migrating layout design data from Altium Designer it is recommended that the Protel format is NOT used as an intermediate format. There are a number of major issues to the Protel output from Altium Designer (for example missing layers, no board outline, figures placed on the incorrect layer) which will result in an invalid design in CADSTAR.

Appendix B - Mapping file

A separate default mapping file is supplied for each Vendor format. This mapping file specifies both the configuration settings to be used and the text mapping for characters not supported in CADSTAR.

The mapping files are currently distributed in the ZIP file with the executable, and should have been unziped into the CADSTAR programs directory as part of the installation. For example:

C:\Program Files\Zuken\CADSTAR 12.1\Programs\ panlink_pads.map
C:\Program Files\Zuken\CADSTAR 12.1\Programs\ panlink_orcad.map

Note: The mapping files will only be placed in the Programs directory for the initial release of the software. They will be placed in the CADSTAR User directory by the installer in future releases.

These files are intended to be edited by the user, however care should be taken as errors and omission in the mapping may cause the designs to fail to be read into CADSTAR.

In the first few sections it is possible to specify which character to use to replace an illegal character in CADSTAR. The supplied mapping files contain default mappings for all the illegal characters in CADSTAR. The format of the mapping is

```
KEY|<original string>|<new string>
```

For example if it is preferred to use "#" to replace "*" in the layer name, then that line in the file should be updated to read:

```
LAYER|*|#
```

The mapping can also be used to rename parts, layers etc as part of the conversion. For example to rename layer "Layer_1" to "Top Elec" the following line should be added:

```
LAYER|Layer_1|Top Elec
```

If it is necessary to match an entire string (eg to avoid partial matching of part names) the initial string should be preceded by "^" and followed by "$". For example a safer way to rename the layer in the previous example would be:

```
LAYER|^Layer_1$|Top Elec
```

Please refer to the later section (in this appendix) for more details on Layer Mapping.

Example extract from a mapping file:

```
#PADS TO CADSTAR EXAMPLE MAPPING FILE

#Replace illegal characters in part, alternate and symbol name.
```

```
VIEW|\|_
VIEW|*|_
...
PARTVIEW|!|_
PARTVIEW|#|_
...
CELL|\|_
CELL|*|_
...
#Replace illegal characters in net name.
NET|\|_
NET|*|_
...
#Replace illegal characters in layer name.
LAYER|\|_
LAYER|*|_
...

#Additional text and figures that may be on the board outline layer
#need to be reassigned to another layer.
LAYER|^Board Outline@LINES$|Board Outline Documentation
LAYER|^Board Outline@TEXT$|Board Outline Documentation
LAYER|^Board Outline@COPPER$|Board Outline Misc
LAYER|^Board Outline@KEEPOUT$|Board Outline Misc

#Design Migration settings
CADSTAR_WRITER|SCALE_CPA|1.0
CADSTAR_WRITER|SCALE_CSA|100.0
CADSTAR_WRITER|MIN_LINE_WIDTH|2540
CADSTAR_WRITER|MIN_OUTLINE_WIDTH|254
CADSTAR_WRITER|MIN_ROUTE_WIDTH|2540
CADSTAR_WRITER|ROUTE_TOLOLERANCE|1270
CADSTAR_WRITER|OFFSET_INDENT|100000
```

Design Migration settings

The Design Migration Tool has a number of settings that may be overridden in the mapping file. If these settings are not specified then internal default values will be used.

Setting	Used	Default value	Description
SCALE_CPA	PCB	1.0	**WARNING: This setting should not be changed by the user!** This is any additional scaling that needs to be applied to the PCB design in addition to the automatic scaling specified in the source design file.

SCALE_CSA	Sch	1.0	This is any scaling that needs to be applied to the Schematic design to ensure that it is correctly displayed in CADSTAR. Note: Terminal symbols are currently generated at a fixed size, so the design may need to be scaled to match that size.
MIN_LINE_WIDTH	Both	2540 DSU	This is the minimum line width to be used for open shapes (eg Schematic lines, PCB figures). Any narrower (or zero) width lines in the source data will be set to this width.
MIN_OUTLINE_WIDTH	Both	254 DSU	This is the minimum line width to be used for closed shape outlines (e.g. PCB figures and copper). CADSTAR will only draw filled copper when the outline width is greater than zero.
MIN_ROUTE_WIDTH	PCB	2540 DSU	This is the minimum line width to be used for PCB routes. Any narrower (or zero) width routes in the source data will be set to this width.
ROUTE_TOLOLERANCE	PCB	1270 DSU	This is the distance between a route and a point on the PCB that the tool will be considered to be connected. E.g. if in the source data a route does not end exactly on a pad or via, is it is within this distance of the pad/via origin then it will be considered to be connected.
OFFSET_INDENT	Both	10,0000 DSU	To enable symbols to be more easily edited the bottom left corner of the symbol will be shifted by this value (on both the X and Y axis) away from the bottom-left corner of the design space.

IGNORE_UNUSED_SYMBOLS	Both	No	If this setting is present in the mapping file then only PCB and Schematic symbols that are present in the PCB or Sheet will be migrated. Use this setting if the Design Migration process is failing due to errors in symbols that are not needed. Note: This setting requires no value to be specified.
IGNORE_UNUSED_PAD_DEFINITIONS	PCB	No	If this setting is present in the mapping file then only Pad and Via definitions that are used in the PCB design will be migrated. Use this setting if the Design Migration process is failing due to exceeding the CADSTAR limit of 256 Via Codes. Note: This setting requires no value to be specified.

Copper Pour Template settings

The CADSTAR Design Migration Tool will now create copper pour template shapes from both PADS and OrCAD design data. However the Copper Pour Template settings for clearance width, additional isolation, sliver width and thermal relief are not migrated from the source data.
These template settings will be set to default values in the migrated design. If alternative values are required then these can be set in the mapping file and will apply to all copper pour templates in the design.

Setting	**Used**	**Default value**	**Description**
TEMPLATE_CLEARANCE_WIDTH	PCB	25400 DSU	The template setting for clearance width to be used for all copper pour templates.
TEMPLATE_ADD_ISOLATION	PCB	12700 DSU	The template setting for additional isolation to be used for all copper pour templates.
TEMPLATE_SLIVER_WIDTH	PCB	25400 DSU	The template setting for sliver width to be used for all copper pour templates.

TEMPLATE_PAD_ANGLE	PCB	45	The template setting for thermal relief angle on pads to be used for all copper pour templates.
TEMPLATE_VIA_ANGLE	PCB	45	The template setting for thermal relief angle on vias to be used for all copper pour templates.

Layer Mapping

The CADSTAR Design Migration Tool will create layers in CADSTAR that correspond to the layer names specified in the source vendor data. It will also try to set the correct layer usage based on the layer name. Therefore it may be necessary to set up layer mapping in the mapping file if:

1) A different layer name is required.
2) A different layer usage is required.
3) Two (or more) layers in the source data are to be used as the same layer in CADSTAR.

See the syntax described at the start of this section for details on how to specify the layer mapping.

For Example:

1) A different layer name is required.
```
LAYER|^Layer_1$|Top Elec
```

2) A different layer usage is required.
```
LAYER|^Misc_13$|Top Placement
```

3) Two (or more) layers in the source data are to be used as the same layer in CADSTAR.
```
LAYER|^Silk_1_1$|Top Silk
LAYER|^Silk_1_2$|Top Silk
```

The CADSTAR Design Migration Tool will attempt to recognize the layer usage (using a case insensitive comparison) as follows:

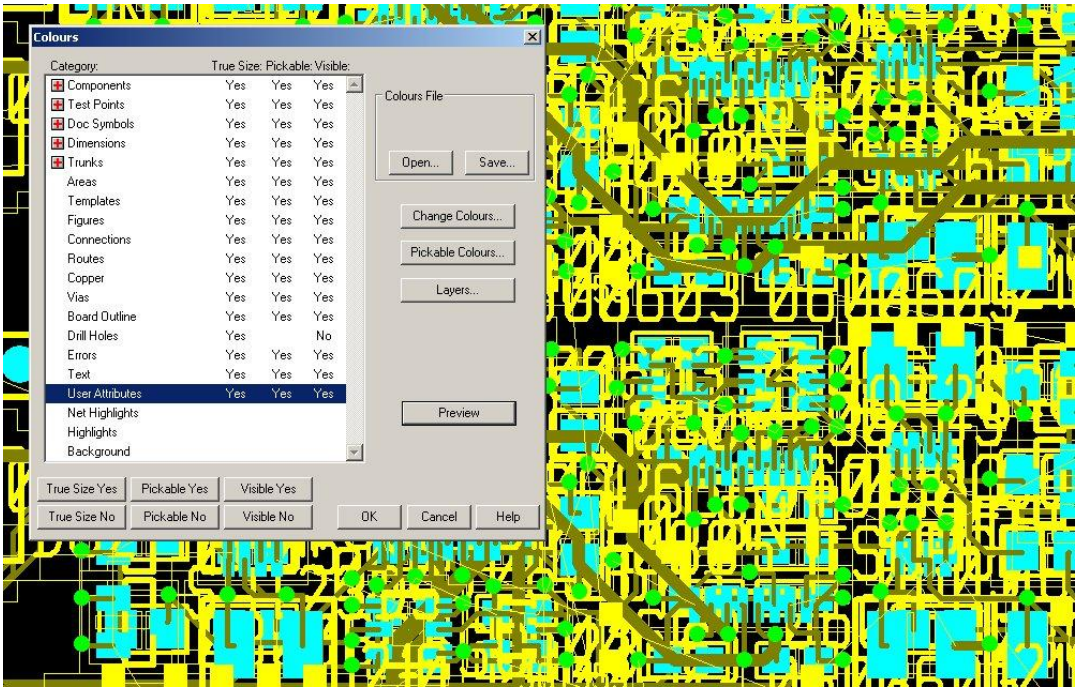
Layer Name	**CADSTAR derived Layer Usage**
BOARD BOARD_OUTLINE BOARD OUTLINE BOARD_FIGURE	BOARD OUTLINE (May only contain a single figure plus cutouts.)
SOLDER	SOLDERRESIST
PASTE	PASTE
PLACE	PLACEMENT

SILK	SILKSCREEN
ROUT *KEEP*	ROUTING
All unmatched layers	DOCUMENTATION

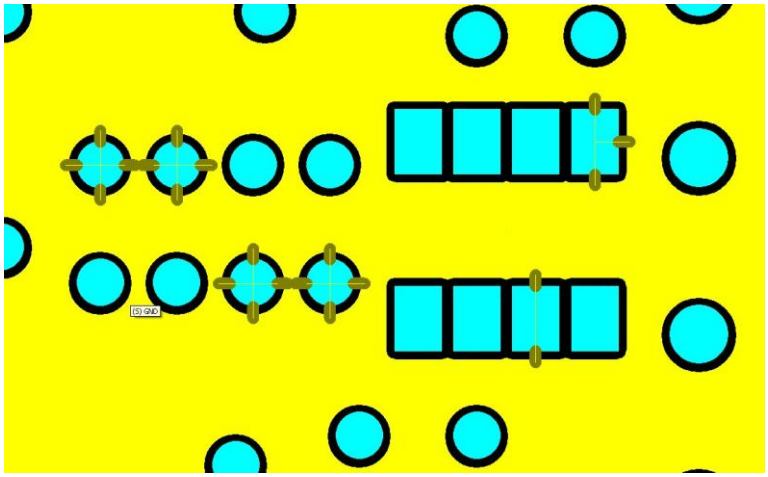
Appendix C - Known issues and limitations

The following are known issues and limitations with the current release of the tool.

1. Attributes that are not visible in the source data are visible in CADSTAR. This is necessary to enable the correct transfer of the attributes. The display of these attributes can be disabled by using the **Colours** dialog in CADSTAR.



2. On PCB designs, CADSTAR may report unresolved connections for routes used as thermal connections to pads.



3. Pad names that exceed the maximum pad name length in CADSTAR will be replaced with the simple default name “Pad <N>”.
   Note: In some vendor formats pads are not named, so the tool will attempt to generate names based on the pad details, however this is likely to exceed CADSTAR length limits, so the short default name will be used instead.

```
WAR Pad name 'PS_-2 2286 R   1409-1 2286 R0  2286 R25 3048 R' exceeds
maximum limit, replacing name with 'Pad 1'.
WAR Pad name 'PS_-2 5715 R   4762-1 5715 R0  5715 R25 6477 R' exceeds
maximum limit, replacing name with 'Pad 2'.
```

4. Terminal and connection symbols on schematic sheets are currently hard-coded to be a fixed size and shape. Connection symbols (eg “Terminal”, “Junction Point” and “Dangler”) are frequently specific to CADSTAR and are automatically created by the Design Migration Tool. Any definitions of such symbols in the source data are ignored.

5. User defined pads with an arbitrary shape are not currently supported by the Design Migration Tool. Pad shapes that are not recognised as one of the standard pad shapes (round, square, finger, bullet, rectangle and annulus) are converted to a rectangle with a size equal to the bounding box of the pad figure. This may mean that the resulting pad shape is now in error with nearby copper or routes. It is recommended that an Electrical Rules check is run in CADSTAR if arbitrary shapes are used in the source design.

```
ERR Unrecognized pad shape for 'Pad 1' on layer 'Layer_1'(creating
dummy pad).
ERR Unrecognized pad shape for 'Pad 1' on layer 'Layer_4'(creating
dummy pad).
```

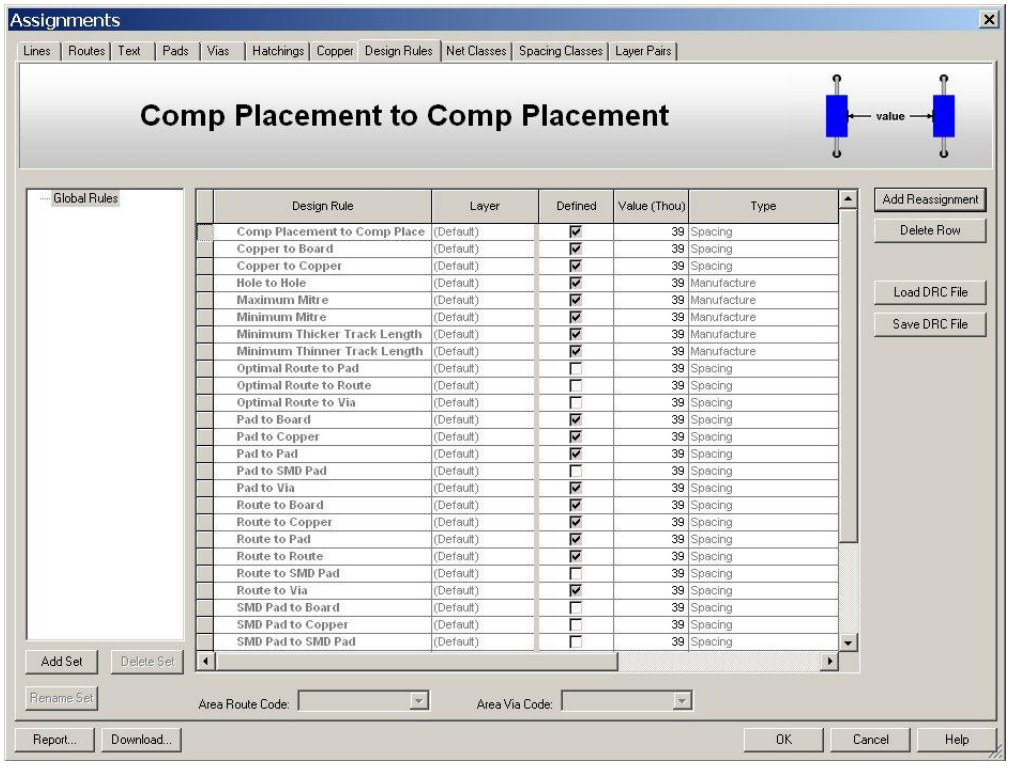
6. Parts that have two schematic pins mapped to the same package pin are not currently translated correctly. CADSTAR does not support common pin definitions so it is not possible to recreate these parts exactly. It recommended that these parts be changed in the source data before using the Migration Tool.
   This issue may also be seen where multiple package pins are mapped to the same power or ground signal.

```
Warning: Part definition 'MyPart123' has more than one pin pointing
to terminal 9 on gate 'A'
Warning: Part information for part MyPart123' has not been loaded
because of errors in its definition. Part should be reloaded from
library.
```

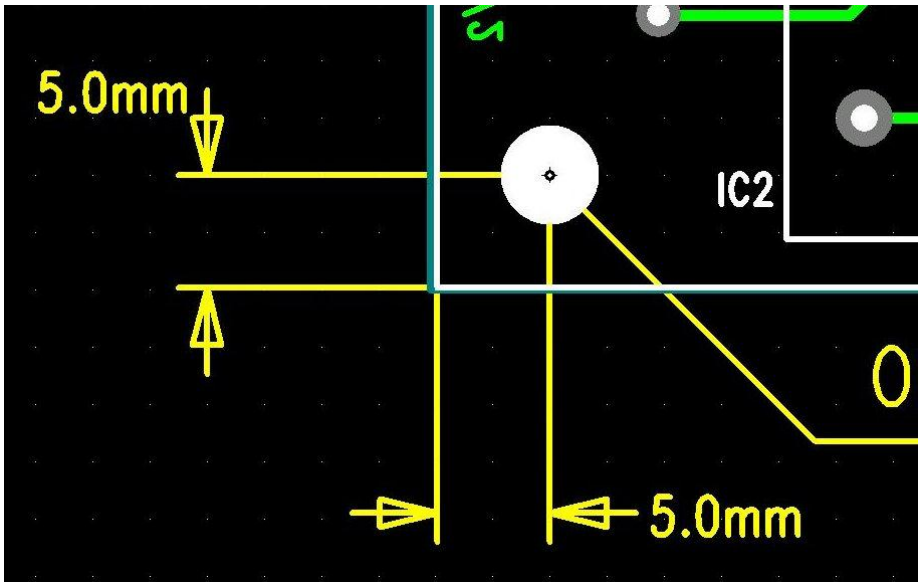
7. In PCB designs where two or more parts share a common footprint, in some cases the Design Migration Tool may currently fail to identify the correct part. To enable the migration process to complete the first part that references the footprint will be selected by default. It will be necessary to manually change the part to be the correct part after the migration is complete.
   The Design Migration Tool may also fail to identify the correct part where a part has been inconsistently named between the schematic and layout source designs.

```
WAR Could not find the correct part reference for pcb instance 'RN23',
defaulting to '1RNS/10K/8P/ISO/5%/0603X4'.
WAR Could not find the correct part reference for pcb instance 'L1',
defaulting to 'C-10NF/10%/100V/X7R/0603_55288'.
```

8. Design Rules are not currently supported by the Design Migration Tool. When a design is migrated all Design Rules will be set to the CADSTAR default values. It is necessary to manually set these rules before running an Electrical Rules Check.



9. Dimensioning is not currently supported by the Design Migration Tool. Any dimensioning figures or text in the source design will be ignored.



10. Variants are not supported in the Design Migration Tool. There are no plans to support the transfer of any Variant data at this time.

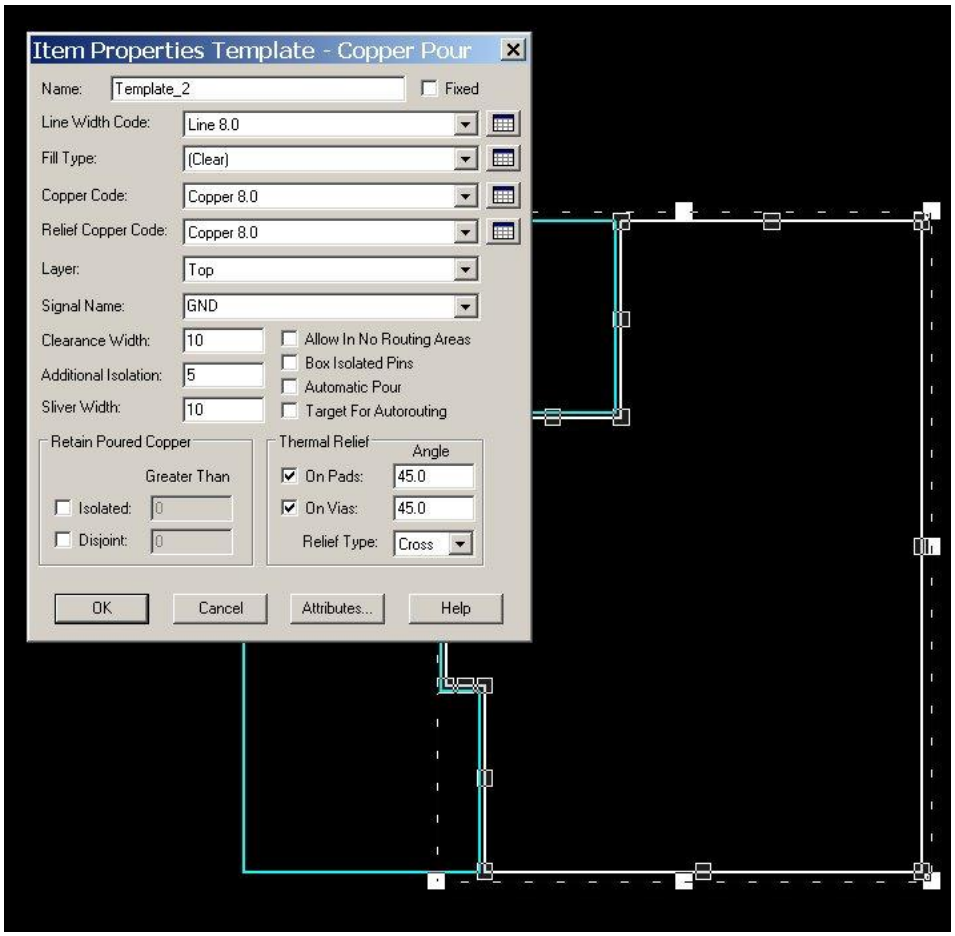
11. Testpoints are not currently supported when migrating from OrCAD Layout designs. It is planned to address this in a future release of the software.

```
Error: Component pin TP13-1 does not exist.
Error: Component pin TP15-1 does not exist.
```

12. Testpoints may not be migrated in P-CAD Layout designs. CADSTAR only supports testpoints that are defined on a single layer. It may not be possible to determine this layer from the design data.

```
WAR Unable to process pad 'P:EX80Y80D501' on net 'TRIAC_MT2_P_2',
testpoint pads connected on internal layers are not supported in
CADSTAR.
WAR Unable to process pad 'P:EX80Y80D501' on net 'TRIAC_MT2_P',
testpoint pads connected on multiple layers are not supported in
CADSTAR.
```

13. Copper Pour Template settings for clearance width, additional isolation, sliver width and thermal relief are not migrated from the source data. The CADSTAR Design Migration Tool will now create copper pour template shapes from both PADS and OrCAD design data but it does not migrate any data for these template settings. The template settings will be set to default values in the migrated design. If alternative values are required then these can be set in the mapping file and will apply to all copper pour templates in the design. (See the mapping file section for more details.)



Limitations when migrating Altium Designer data

When migrating layout design data from Altium Designer it is recommended that the P-CAD format (rather than Protel) is used as an intermediate format. However there are limitations in the P-CAD output from Altium Designer that will affect the migration:

1. Copper pour templates are migrated in the CADSTAR Design Migration Tool, however the associated poured copper may not be migrated. It may be necessary to re-pour any copper once a layout design has been migrated.

2. Holes in footprint figures that are not part of a padstack are not currently migrated. For example mounting holes in P-CAD are represented as a figure on the board layer within the footprint symbol. It is planned to address this in a future release of the software.

When migrating layout design data from Altium Designer it is recommended that the Protel format is NOT used as an intermediate format. There are a number of major issues

with the Protel output from Altium Designer which will result in an invalid design in CADSTAR. For example:

1. The board outline will not be migrated
2. The layer stack will be missing layers
3. Figures will be placed on incorrect layers.
4. Poured copper may be migrated as an outline only.
5. Part data is not migrated.
6. Part properties are incorrectly placed.